

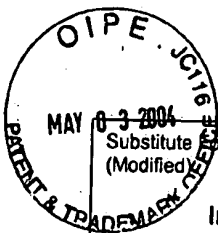
Substitute Form PTO-1449 (Modified) DEC 29 2000 INFORMATION DISCLOSURE STATEMENT by Applicant (Use several sheets if necessary) (37 CFR 1.102(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-596001	Application No. 09/941,158
	Applicant William R. Wheeler et al.		
	Filing Date August 28, 2001	Group Art Unit 2812	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
<i>W</i>	AA	5,220,512	06/1993	Watkins, et al.			
	AB						
	AC						
	AD						
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Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
<i>W</i>	AL	0 433 066	06/1991	EPO				
<i>W</i>	AM	1 065 611	01/2001	EPO				
<i>W</i>	AN	WO00/65492	11/2000	WIPO				
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AQ	
	AR	
	AS	
	AT	

Examiner Signature <i>W. R. Wheeler</i>	Date Considered 5/13/04
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Patent and Trademark OfficeAttorney's Docket No.
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(Use several sheets if necessary)

(37 CFR §1.98(b))

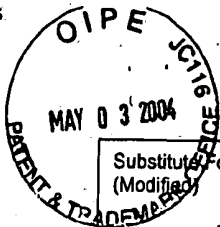
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2812**U.S. Patent Documents**

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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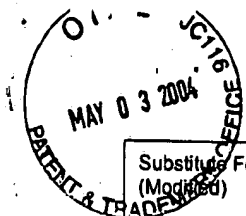
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2812**U.S. Patent Documents**

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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ABBB		6,490,545	12/2002	Peng			

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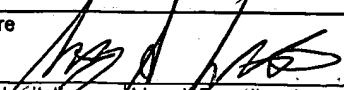
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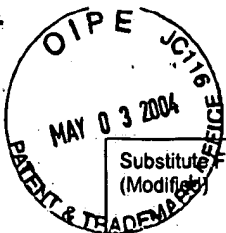


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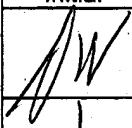

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	AOOO	2003/0177455	09/2003	Kaufman, et al.			


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W	APPP	0 404 482	12/1990	EPO				
	AQQQ	0 720 233	07/1996	EPO				
	ARRR	0 901 088	03/1999	EPO				
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	AVVV	08-314892	11/1996	Japan				
	AWWW	2001-068994	03/2001	Japan				
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	AYYY	WO 98/55879	12/1998	WIPO				
	AZZZ	WO 99/39268	08/1999	WIPO				

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	AAAAA	Gassenfeit, E. H., "Control System Design Realization via VHDL-A: Requirements", Proceedings of the 1996 IEEE International Symposium on Computer-Aided Control System Design, September 15, 1996, pp. 282-285.
	ABBBB	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.
	ACCCC	Lahti, et al., "SADE: a Graphical Toll for VHDL-Based System Analysis", 1991 IEEE International Conference on Computer-Aided Design, November 11, 1991, pp. 262-265.
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	AEEEE	Maxfield, C., "Digital Logic Simulation: Event-Driven, Cycle-Based, and Home-Brewed", <i>Electrical Design News</i> , 41(14):129-136 (1996).
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	AHHHH	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.
	AIIII	NN9407481, "Functional Modeling using object Collaboration Diagram", IBM Technical Disclosure Bulletin, Vol. 37, No. 7, July 1994, pp. 481-486.
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	ALLLL	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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